JC10 Rec'd PCT/PTO 04 JAN 2002

FORM PTO-1390 (REV 11-2000)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 117-375

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5): 10/019686

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/GB00/02571	05/07/2000	08/07/1999

TITLE OF INVENTION

PRINTED CIRCUIT FABRICATION

APPLICANT(S) FOR DO/EO/US

BAND, C.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☐ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has **NOT** expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 To 20 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information. PTO Form 1449, Intl Srch Report, Cited Refs

589889

10/019686 531 Rec'd PCT/PTO 04 JAN 2002

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
unknown	PCT/GB00/02571	117-375

21. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):		
-- Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO.....$1040.00		
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....$890.00		
-- International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO.....$740.00		
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....$710.00		
-- International preliminary examination fee (37 C.F.R. 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4).....$100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE			
Total Claims	17	-20 =	0	X	$18.00	$ 0.00	
Independent Claims	3	-3 =	0	X	$84.00	0.00	
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)					$280.00	$ 0.00	
CLAIM FEES ARE NOT BEING PAID AT THIS TIME				**TOTAL OF ABOVE CALCULATIONS =**		$ **1020.00**	

☒ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.	510.00	
SUBTOTAL =	$ **510.00**	
Processing fee of $130.00, for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +	0.00	
TOTAL NATIONAL FEE =	$ **510.00**	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). **$40.00** per property +	$ 0.00	
Fee for Petition to Revive Unintentionally Abandoned Application ($1280.00 -- Small Entity = $640.00)	$ 0.00	
TOTAL FEES ENCLOSED =	$ **510.00**	
	Amount to be: refunded	$
	Charged	$

a. ☒ A check in the amount of $510.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 14-1140 in the amount of $_____ to cover the above fees. A duplicate copy of this form is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 14-1140. A duplicate copy of this form is enclosed.
d. ☒ The entire content of the foreign application(s), referred to in this application is/are hereby incorporated by reference in this application.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

NIXON & VANDERHYE P.C.
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SIGNATURE

Arthur R. Crawford
NAME

25,327 REGISTRATION NUMBER

January 4, 2002 Date

589889

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

BAND, C. Atty. Ref.: 117-375

Serial No. unknown Group:

Filed: January 4, 2002 Examiner:

For: PRINTED CIRCUIT FABRICATION

* * * * * * * * * * *

January 4, 2002

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

In order to place the above-identified application in better condition for examination, please amend the application as follows:

IN THE SPECIFICATION

Please substitute the following paragraphs in the specification for corresponding paragraphs previously presented. A copy of the amended specification paragraphs showing current revisions is attached.

Page 1, before the first line, insert as a separate paragraph:

This application is the US national phase of international application PCT/GB00/02571 filed 05 July 2000, which designated the US.

IN THE CLAIMS

Please substitute the following amended claims for corresponding claims previously presented. A copy of the amended claims showing current revisions is attached.

4. A method according to claim 1 wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

5. A method according to claim 1 wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

6. A method according to claim 1 wherein the etch band is less than about 30 microns wide.

7. A mask for use in producing a resist pattern for etching of a printed circuit, the mask being produced by the method of claim 1.

10. A printed circuit according to claim 8 wherein the etch band is of substantially the same width as the narrowest conductor or the narrowest separation between conductors in the printed circuit

11. A printed circuit according to claim 8wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

12. A printed circuit according to claim 8 wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

13. A printed circuit according to claim 8 wherein the etch band is less than 30 microns wide.

16. A method according to claim 14 wherein the pattern includes conductor elements spaced by less than about 30 microns.

17. A method according to claim 14 wherein the regions of constant width are of substantially the same width as the narrowest element or narrowest separation between elements in the printed circuit.

REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made**."

Respectfully submitted,

NIXON & VANDERHYE P.C.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Page 1, before the first line, insert as a separate paragraph:

This application is the US national phase of international application PCT/GB00/02571 filed 05 July 2000, which designated the US.

IN THE CLAIMS

4. A method according to claim 1~~, 2 or 3~~ wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

5. A method according to claim 1~~, 2, 3 or 4~~ wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

6. A method according to ~~any one of the preceding~~ claims 1 wherein the etch band is less than about 30 microns wide.

7. A mask for use in producing a resist pattern for etching of a printed circuit, the mask being produced by the method of ~~any one of the preceding~~ claims 1.

10. A printed circuit according to claim 8 ~~or 9~~ wherein the etch band is of substantially the same width as the narrowest conductor or the narrowest separation between conductors in the printed circuit

11. A printed circuit according to claim 8~~, 9 or 10~~ wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

12. A printed circuit according to claim 8~~,9, 10 or 11~~ wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

13. A printed circuit according to ~~any one of~~ claims 8 ~~to 12~~ wherein the etch band is less than 30 microns wide.

16. A method according to claim 14 ~~or 15~~ wherein the pattern includes conductor elements spaced by less than about 30 microns.

17. A method according to claim 14~~, 15 or 16~~ wherein the regions of constant width are of substantially the same width as the narrowest element or narrowest separation between elements in the printed circuit.

~~18. A mask or a printed circuit substantially as hereinbefore described with reference to and as illustrated in figures 1 and 3 of the accompanying drawings.~~

~~19. A method of producing a mask or a printed circuit substantially as hereinbefore described.~~

PRINTED CIRCUIT FABRICATION

The present invention relates to the fabrication of printed circuits and in particular to methods of producing such printed circuits by etching a desired conductor pattern into a layer of conductive material on a substrate.

Printed circuit boards which consist of a pattern of conductive material, usually copper, on a substrate, such as a resin board, are well known and widely used in the electronics industry. Conventional methods for producing such printed circuits involve the preparation of a uniform layer of conductive material, usually copper, on a support, such as the resin board (though flexible supports are increasingly being used), the desired conductor pattern then being etched into the conductive material. This etching process involves first putting a mask of resist in the desired pattern on the conductive material and then spraying the conductive layer with an etchant to remove those areas of the conductor which are not masked by the resist. The pattern of resist is conventionally produced by laying down a uniform layer of photo resist, which is then exposed to a pattern of UV light corresponding to the desired circuit pattern (or its negative). Areas of the resist which have been exposed (or not exposed in the negative process) are then dissolved away. Usually the pattern of UV light is created by using a mask, or photographic master, which itself is in the pattern of the desired printed circuit or its negative. Such masks can be produced by various techniques such as laser plotting or conventional photography.

With the miniaturisation of electronic devices printed circuits of finer and finer resolution are required all the time. At the moment printed circuits having a fine resolution include conductors of widths as narrow as 150 microns. However, there is a need for printed circuits with conductors much narrower than this, down to 30 microns or below, even in the range 10 to 12 microns. A problem with producing such fine circuits is that the circuits often contain imperfections, such as the narrowest conductors being of varying width, or even broken. This places limits on the fineness of the resolution which can be achieved.

The present invention provides an improved method for producing printed

circuit boards in which the problems associated with producing very narrow conductor elements when etching a printed circuit are reduced. In particular the present invention proposes that the conductor elements of the circuit should be delineated by etched regions of constant width. In other words, they should be separated from regions of unused conductor by a constant width etch band. This means that, as compared with a conventional printed circuit, there will be large areas of unused conductor (e.g. copper) left on the circuit board. Conventionally all such unused areas would be etched away. However with the present invention they are left on the printed circuit board, and just separated from the conductors by the constant width etch bond.

Thus the present invention involves a modification to the method of producing the mask which is used to define the resist pattern for the etching process. The mask is designed so that the desired printed circuit pattern is delineated by a constant width etch band.

The etch band is preferably of the same width of the narrowest conductor separation or conductor in the printed circuit. It is particularly useful where the printed circuit conductor pattern includes conductor regions less than about 30 microns wide or spaced by less than about 30 microns.

With the present invention the same amount of conductor needs to be etched away along all conductor elements. With a conventional printed circuit board some areas where the conductors are very closely spaced will require less copper to be etched away than areas where there are very few conductors, or whether conductors are widely spaced. It is this difference in the amount of conductor which needs to be etched away which causes variations in etch rate. The local etch rate varies according to the amount of local conductor which has to be etched away. Because with the present invention the amount of local conductor which has to be etched away is constant (because it consists of a constant width etch band delineating the conductors) the etch rate is the same over the whole pattern. Thus the width of the conductors which are produced is relatively constant and problems of undue narrowing of conductors, undercutting of conductors by etchant, and breaking of conductors are reduced.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings in which:-

Figure 1 illustrates schematically a conventional printed circuit pattern;

Figure 2 illustrates the corresponding pattern according to the present invention; and

Figure 3illustrates at a magnified scale an actual mask produced by an embodiment of the present invention.

Figure 1 shows schematically a very simply printed circuit which the present invention can be applied. Figure 1 illustrates the circuit in conventional form and figure 2 illustrates the modification according to the invention. As can be seen in figure 1 the printed circuit is defined on a substrate 1 and consists of a set of parallel conductors 3a, 3b and 9 of which the conductors 3a and 3b lead to contact pads 5 and the conductor 9 leads off to another region of the printed circuit. It can be seen that the spacing between the conductors varies across the pattern, it being narrow in regions 6 where the conductors are parallel and closely spaced, while being wider in regions 7 and 11 near the contact pads and the edge of the printed circuit. It can also be seen that the conductor 3a has on one side a very narrow spacing to the neighbouring conductor 3b and on the other side a very wide area where all conductor has been etched away. Similarly the conductor 9 has, in region 11, areas on both sides where much conductor has been etched away. Where this pattern is produced at fine resolutions, such as the conductors being of 30 microns width or less, e.g. 10 to 12 microns, it is found that the width of the conductors produced varies in the different regions 6, 7 and 11. The etch rate would be lower in the regions 6 compared to the widely spaced regions 7 and 11. Thus given a constant etching time, the conductors would narrow (because of increased etching) in the regions approaching the contact pads or where the conductor extends to other parts of the printed circuit as at 11.

The present invention solves this problem by modifying the pattern of conductor which is produced in the etching process. The result of this modification is illustrated in figure 2. It can been seen that each of the conductor elements is now surrounded by a constant width etch band 20. The conductor elements are therefore

separated from unused regions of conductor 22 by this constant width band. Thus the amount conductive material which needs to be etched away is now constant over the whole area of the illustrated pattern. This means that the etch rate will be the same over the whole pattern, and variations in width of the conductors produced will be much smaller.

Of course although figure 2 illustrates that only the constant width etch band 20 is etched away, it may be that there are remote regions of the printed circuit substrate which can be etched away without affecting the etch rate locally around the conductors. The invention is concerned with producing a constant etch rate around the conductor elements. Thus given a printed circuit product it may be that only certain regions need to include the constant width etch band delineating the conductors. Edge regions or regions which do not include fine conductors may be produced in a conventional way.

It will be appreciated that in a region where the conductors consist of parallel closely spaced elements, to enable the etch rates to be the same as the etch rate between such elements, the etch band must be of the same width as the spacing between the conductor elements. Often a constant mark-to-space ratio is used which means that the etch band can be of the same width as the narrowest conductor on the board.

Figure 3 is a magnified view of an actual mask designed according to an embodiment of the invention. The white areas correspond to areas of conductor which will be left on the printed circuit. Thus there are a plurality of contact pads 5 which are connected by conductor elements or "wires" 3 to another row of contact pads 4. In addition to these conductor elements it can be seen that there are large areas of unused conductor 15 which are left because the conductor pattern is delineated by the constant width etch band 10. The constant width etch band is of the same width of the separation between the conductors in the region 17 where they are narrowly spaced.

While the present invention has been described as being applied in the design of the mask for using the etching process, it will of course be appreciated that it can be applied however the selective etching of conductor is achieved. Thus, for

instance, it may be that the uniform layer of resist is illuminated in a scanning process, rather than by using a mask, or is written directly by a light beam. Alternatively the resist pattern may be produced by other means. However the present invention is still applicable in that the pattern of resist must define a constant width etch band delineating the desired conductor regions in the pattern.

CLAIMS

1. A method of producing a mask for use in producing a resist pattern for etching of a printed circuit, comprising defining in the mask a constant width etch band delineating the desired printed circuit conductor pattern.

2. A method according to claim 1 wherein the etch band is of substantially the same width as the narrowest conductor or the narrowest separation between conductors in the printed circuit.

3. A method according to claim 1 wherein the etch band separates the desired printed circuit conductor pattern from regions of unused conductor on the printed circuit.

4. A method according to claim 1, 2 or 3 wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

5. A method according to claim 1, 2, 3 or 4 wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

6. A method according to any one of the preceding claims wherein the etch band is less than about 30 microns wide.

7. A mask for use in producing a resist pattern for etching of a printed circuit, the mask being produced by the method of any one of the preceding claims.

8. A printed circuit in which the printed circuit elements are delineated by a constant width etch band.

9. A printed circuit according to claim 8 in which the etch band separates

the printed circuit elements from regions of unused conductor.

10. A printed circuit according to claim 8 or 9 wherein the etch band is of substantially the same width as the narrowest conductor or the narrowest separation between conductors in the printed circuit.

11. A printed circuit according to claim 8, 9 or 10 wherein the printed circuit conductor pattern includes conductor regions less than about 30 microns wide.

12. A printed circuit according to claim 8, 9, 10 or 11 wherein the printed circuit conductor pattern includes conductor regions spaced by less than about 30 microns.

13. A printed circuit according to any one of claims 8 to 12 wherein the etch band is less than 30 microns wide.

14. A method of producing a printed circuit comprising a pattern of conductor elements, the method comprising the steps of: defining on a printed circuit substrate a pattern of resist to leave exposed regions of conductor to be etched away, the exposed regions comprising areas of constant width delineating the conductor elements.

15. A method according to claim 14 wherein the conductor elements include elements less than about 30 microns wide.

16. A method according to claim 14 or 15 wherein the pattern includes conductor elements spaced by less than about 30 microns.

17. A method according to claim 14, 15 or 16 wherein the regions of constant width are of substantially the same width as the narrowest element or narrowest separation between elements in the printed circuit.

18. A mask or a printed circuit substantially as hereinbefore described with reference to and as illustrated in figures 1 and 3 of the accompanying drawings.

19. A method of producing a mask or a printed circuit substantially as hereinbefore described.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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International Bureau

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18 January 2001 (18.01.2001)

PCT

(10) International Publication Number
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(30) Priority Data:
9916060.8 8 July 1999 (08.07.1999) GB

(71) Applicant *(for all designated States except US)*: ISIS INNOVATION LIMITED [GB/GB]; Ewert House, Ewert Place, Summertown, Oxford OX2 7BZ (GB).

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(81) Designated States *(national)*: JP, US.

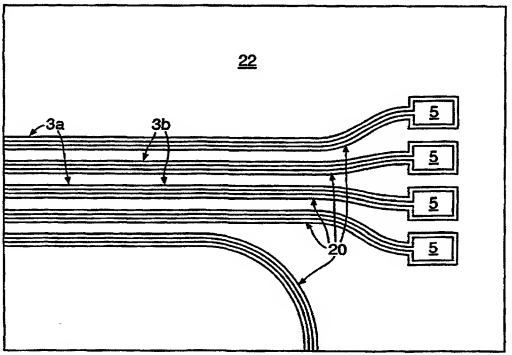
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*

(88) Date of publication of the international search report:
12 July 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PRINTED CIRCUIT FABRICATION



(57) Abstract: A mask for producing a printed circuit board is defined in which the conductor elements of the printed circuit pattern are delineated by a constant width etch band (20). This means that all conductors (3a, 3b, 9) are separated from neighbouring areas of conductive material (22) by the same distance. Thus etch rates across the printed circuit pattern do not vary according to the separation of the conductors (3a, 3b, 9).

Fig.1.

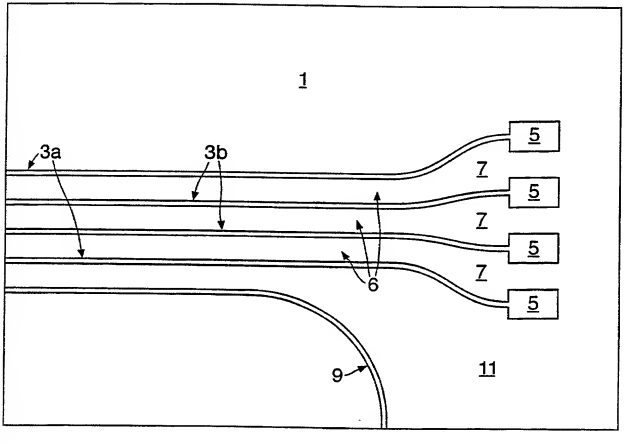


Fig.2.

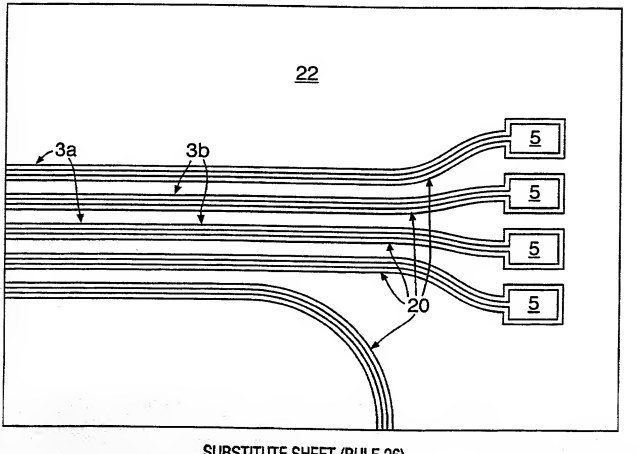
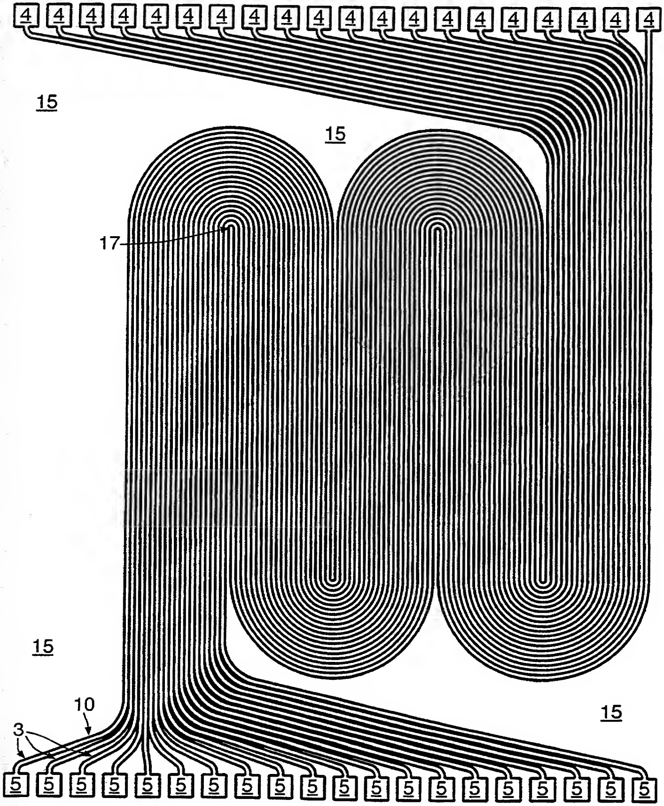


Fig.3.



RULE 63 (37 C.F.R. § 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As below named inventor(s), I/we hereby declare that

This declaration is of the following type:

☐ original	☐ design	☐ supplemental
☒ national stage of PCT		
☐ divisional	☐ continuation	☐ continuation-in-part

My/our residence, post office address and citizenship are as stated below next to my/our name.

I/we believe I/we am/are the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PRINTED CIRCUIT FABRICATION

the specification of which (check one)

☐ is attached hereto

☐ was filed on _____
in the United States Patent and Trademark Office as Application Serial No. _____
and was amended on _____ *(if applicable)*

☐ was described and claimed in PCT International Application No. **PCT/GB00/02571**
filed on **5 Jul 2000**
and as amended under PCT Article 19 on _____ *(if any)*

I/we hereby state that I/we have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I/we acknowledge the duty to disclose information which is material to patent ability as defined in 37 C.F.R. § 1.56.

I/we hereby claim foreign priority benefits under 35 U.S.C §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or under § 365(a) of any PCT International Application(s) which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or PCT International Application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119

Application No.	Country	Filing Date	Priority Claimed	
			Yes	No
9916060.8	GB	8 Jul 1999	X	
PCT/GB00/02571		5 Jul 2000		

I/we hereby claim the benefit under 35 U.S.C. § 119(e) of any United States Provisional Application(s) listed below:

UNITED STATES PROVISIONAL APPLICATION(S)

Application No.	Filing Date

I/we hereby claim the benefit under 35 U.S.C. § 120 of any United States Application(s) or § 365(c) of any PCT International Application(s) designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International Application in the manner provided by the first paragraph of 35 U.S.C. § 112, I/we acknowledge the duty to disclose information which is material to patent ability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior applicat ion and the national PCT international filing date of this application.

PRIOR UNITED STATES/PCT INTERNATIONAL APPLICATION(S)

Application No.	Filing Date	Status (patented, pending/abandoned)
PCT/GB00/02571	5 Jul 2000	

And I hereby appoint **Nixon & Vanderhye P.C., 1100 North Glebe Road, 8th Floor, Arlington, Virginia 22201-4714, telephone number (703) 816-400 (to whom all communications are to be directed)**, and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009; Duane M. Byers, 33363; Paul J. Henon, 33626; Jeffry H. Nelson, 30481; John R. Lastova, 33149; H. Warren Burnam, Jr., 29366; Thomas E. Byrne, 32205.

I/we hereby declare that all statements made herein of my/our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C § 1001 and that such willful false statements may jeopardise the validity of the application or any patent issued thereon.

COMBINED DECLARATION AND POWER OF ATTORNEY

x C W Band -	09-01.2002
Inventors Signature	Date

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